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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,495	09/24/2001	Hiroyuki Amishiro	50090-338	5812

7590 04/14/2005

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EXAMINER	
BLUM, DAVID S	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SRM

Office Action Summary	Application No.	Applicant(s)	
	09/960,495	AMISHIRO ET AL.	
	Examiner	Art Unit	
	David S. Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *14-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,11 and 22* is/are rejected.

7)☒ Claim(s) *4,6-10 and 21* is/are objected to.

8)☒ Claim(s) *1-22* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the amendment filed 12/07/04.

DETAILED ACTION

Drawings

The objection to Figure 8 is withdrawn. The applicant has stated for the record (remarks filed 12/07/04) that part 7 of figure 7 is the same part (unnumbered) now surrounded by part 3 of figure 8.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by 4,384,299 to Raffel et al.

In reference to Claim 1, Raffel et al. teaches:

• a semiconductor device having a plurality of resistor elements (100) formed on an element isolating insulating film (114 and 102) in predetermined regions on a surface of a semiconductor substrate (110), said semiconductor device comprising active regions (106) proximate to each of said resistor elements (100), wherein said active regions

(106) are formed in said semiconductor substrate (110) and partition said element isolating insulating film (114) between adjacent resistor elements (100) (See Figure 9).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351 (a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,365,481 to Bonser et al.

In reference to Claim 1, Bonser et al. teaches:

• a semiconductor device (10) having a plurality of resistor elements (30 and 32) formed on an element isolating insulating film (16) in predetermined regions on a surface of a semiconductor substrate (12), said semiconductor device comprising active regions (14) proximate to each of said resistor elements (30 and 32), wherein said active regions (14) are formed in said semiconductor substrate (12) and partition said element isolating insulating film (16) between adjacent resistor elements (30 and 32) (See Figure 1 and column 3 lines 10-53).

In reference to Claim 2, Bonser et al. teaches:

• wherein said element isolating insulating film is formed by shallow trench isolation (See Figure 1 and column 3 lines 10-53).

Furthermore, the Examiner notes that the patentability of a product does not depend on its method of production. Therefore, the limitation that the insulating film is formed by shallow trench isolation carries no patentable weight.

"Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao and Sato et al., 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also In re Brown and Saffer, 173 USPQ 685 (CCPA 1972): In re Luck and Gainer, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and In re Marosi et al., 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a "product by, all of claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear.

In reference to Claim 3, Bonser et al. teaches:

• wherein said plurality of resistor elements are arranged on said element isolating insulating film and wherein said element isolating insulating film under said resistor elements is set to a predetermined width by said active regions (See Figure 1 and column 3 lines 10-53).

In reference to Claim 11, Bonser et al. teaches:

• wherein said active regions extend close to lengthwise ends of said resistor elements which are surrounded by said active regions (See Figure 1 and column 3 lines 10-53)

5. Claims 1, 3, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,285,066 to Meyer.

In reference to Claim 1, Meyer teaches:

• a semiconductor device (10) having a plurality of resistor elements (138) formed on an element isolating insulating film (136) in predetermined regions on a surface of a semiconductor substrate (10), said semiconductor device comprising active regions (76) proximate to each of said resistor elements (138), wherein said active regions (76) are formed in said semiconductor substrate (10) and partition said element isolating insulating film (136) between adjacent resistor elements (138) (See Figures 8 and 13-14 and columns 3-8 lines 05-40).

In reference to Claim 3, Meyer teaches:

• wherein said plurality of resistor elements are arranged on said element isolating insulating film and wherein said element isolating insulating film under said resistor elements is set to a predetermined width by said active regions (See Figures 8 and 13-14 and columns 3-8 lines 05-40).

In reference to Claim 22, Meyer teaches:

• active regions (76) proximate to each of the resistor elements (138), wherein between portions, formed on the element isolation film (136), of adjacent resistor elements, said active regions are formed in said semiconductor substrate and partition said element isolating film between adjacent resistor elements (figures 12-13).

6. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated by US 2002/0004270 to Moriwaki et al.

In reference to Claim 5, Moriwaki et al. teaches:

• a semiconductor device having a plurality of resistor elements (103C or 303C) formed on an insulating film (101, 201 or 301) in predetermined regions on a surface of a semiconductor substrate, said semiconductor device comprising: active regions (105, 106, 305 and 306) proximate to each of said resistor elements, wherein the regions including said active regions are furnished with dummy gate electrodes (10313 and 30313) constituting the same layer as that of said resistor elements (See Figures 1-9 and paragraphs 0063-0106).

Moriwaki does not specifically state that the device contains a plurality of resistors, only that the resistor is in the logic circuit for the MOSFET (transistor). That there is a plurality of transistors and resistors in the device is implicit. Paragraph 0091 refers to a DRAM/LOGIC LSI. One cannot have a logic region without a plurality of transistors (minimum 2), therefore a plurality of accompanied resistors. Further, memory/logic arrays are made in the gigabytes and are readily available on the open market. These arrays would not function on a single MOSFET and resistor. Thus the teachings of Moriwaki on how to make a peripheral MOSFET and internal MOSFET are implicitly toward a plurality of each.

"[I]n considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom." *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968) See also *In re Lamberti*, 545 F.2d 747, 750, 192 USPQ 278, 280 (CCPA 1976).

Allowable Subject Matter

7. Claims 4, 6-10, 12, 13,and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. 2. The following is a statement of reasons for the indication of allowable subject matter. With regard to Claim 4, the prior art of record, in combination with the other claimed features, fails to teach

wherein said insulating film under said resistor elements is set to a predetermined width by said active regions, wherein said predetermined width is defined by an amount of shift in resistance value of said resistor elements, said amount of shift being defined by said predetermined width. With regard to Claims 6-8, the prior art of record, in combination with the other claimed features, fails to teach wherein said dummy gate electrodes entirely cover the active regions, or wherein said active regions are covered with a plurality of dummy
gate electrodes, or wherein a distance between each of said resistor elements and each of said dummy gate electrodes is held constant.

With regards to Claims 9, 10 and 21 the prior art of record, in combination with the other claimed features, fails to explicitly teach wherein a plurality of said resistor elements are furnished between any adjacent two of said active regions.

With regards to Claim 12, the prior art of record, in combination with the other claimed features, fails to explicitly teach wherein the resistor elements are surrounded by the dummy gate electrodes.

With regards to Claim 13, the prior art of record, in combination with the other claimed features, fails to explicitly teach wherein said resistor elements are formed by a layer constituting gate electrodes of MOS transistors furnished outside said predetermined regions.

Response to Arguments

8. Applicant's arguments filed 12/07/04 have been fully considered but they are not persuasive.

The applicant argues that claim 1 is allowable as Raffel does not teach that the resistor element is formed only on the element isolation feature. However, the claim reads "only on the element isolation feature" not "on and in contact with". The resistor element is clearly "only on" as it is not on another part that is not on the element isolation feature. As to the intervening silicon nitride layer, this is also insulating and may be considered the element isolation element, or part of it.

The applicant argues that claim 1 is allowable as Bonser does not teach that the resistor element is formed only on the element isolation feature. However, the claim reads "only on the element isolation feature" but does not contain any further limitations. "Only on" may (as argued) mean only on the element isolation regions and not on any other region. "only on" may also mean on, but not under. Claim language is interpreted in the broadest meanings and thus Bonser reads on the claimed matter.

The applicant argues that claim 1 is allowable as Meyer does not teach that the resistor element is formed on a surface of a substrate but rather in the feature. Claim 1 recites that the resistor elements are formed on an isolating film in predetermined regions of a surface of the semiconductor substrate. The examiner notes that a trench bottom is a surface of the semiconductor substrate.

The applicant further argues that Meyer refers to part 76 as a mesa and not as an active region, thus there is no teaching that the part is later doped to form an active region. However, the background of the invention teaches that field oxides and trenches are used to separate active regions (trenches have little encroachment into the active region). Therefore, the mesas represent active regions separated by the isolation trenches. Active regions have doping to allow device function.

The applicant argues that Babcock (it is believed the applicant meant Moriwaki) does not disclose a plurality of resistors, but only one. Paragraph 0091 refers to a DRAM/LOGIC LSI. One cannot have a logic region without a plurality of transistors (minimum 2), therefore a plurality of accompanied resistors. Further, memory/logic arrays are made in the gigabytes and are readily available on the open market. These arrays would not function on a single MOSFET and resistor. Thus the teachings of Moriwaki on how to make a peripheral MOSFET and internal MOSFET are implicitly toward a plurality of each.

"[I]n considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom." *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968) See also *In re Lamberti*, 545 F.2d 747, 750, 192 USPQ 278, 280 (CCPA 1976).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (703) 872-9306. The facsimile number for customer service is (703)-872-9317.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum
April 12, 2005